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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,896	06/30/2003	Dong-Ho Hyun	SAM-0424	8333

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,896	HYUN ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-30* is/are allowed.

6)☐ Claim(s) *1-3,8,13 and 22* is/are rejected.

7)☒ Claim(s) *4-7,9-12 and 14-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1- 30 are presented in the instant application according to the Applicants' filing on 06/30/2003.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 01/06/2003, which includes the Taiwanese reference Pub. No. 387,065 is in compliance with 37 CFR 1.98. Therefore it has been considered.

Inventorship

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Objections/Minor Informalities

4. Claims 1, 4-7, and 9-29 are objected to because of the following informalities:

For the listed claims below, it is suggested by the examiner to replace "if" with

-- when --, therein, to reflect a positive limitation and not a conditional one.

Claim 1, lines 5 and 2;

Claim 5, line 2;

Claim 7, line 3;

Claim 10, line 2;

Claim 12, line 3;

Claim 13, lines 7, 11, and 13;

Claim 14, line 12;

Claim 17, line 2;

Claim 18, line 2;

Claim 21, line 3; and

Claim 23, lines 7, 10, 12, 16, 18, 21, and 23.

Claim 4, lines 3 and 6, insert -- , -- after "transistor" is suggested for clarification.

Claim 6, lines 3 and 6, insert -- , -- after "transistor" is suggested for clarification.

Claim 9, lines 3 and 5, insert -- , -- after "transistor" is suggested for clarification.

Claim 11, lines 3 and 5, insert -- , -- after "transistor" is suggested for clarification.

Claim 14, lines 3, 5 and 8, insert -- , -- after "transistor" is suggested for clarification.

Claim 15, line 3, insert -- , -- after "transistor" is suggested for clarification.

Claim 16, lines 3 and 6, insert -- , -- after "transistor" is suggested for clarification.

Claim 18, lines 3, 5 and 8, insert -- , -- after "transistor" is suggested for clarification.

Claim 19, line 3, insert -- , -- after "transistor" is suggested for clarification.

Claim 20, lines 3 and 6, insert -- , -- after "transistor" is suggested for clarification.

Claim 24, lines 3, 5 and 8, insert -- , -- after "transistor" is suggested for clarification.

Claim 25, line 1, replace "14" with –24--, therein, for proper claim dependency;

lines 2 and 4, insert -- , -- after "transistor" is suggested for clarification.

Claim 26, lines 3 and 6, insert -- , -- after "transistor" is suggested for clarification.

Claim 27, lines 3, 5 and 8, insert -- , -- after "transistor" is suggested for clarification.

Claim 28, lines 3 and 5, insert -- , -- after "transistor" is suggested for clarification.

Claim 29, lines 3 and 6, insert -- , -- after "transistor" is suggested for clarification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-3, 8, 13 and 22 are rejected under 35 U.S.C. 102(a) as being anticipated by Kim (KR Pub. No. 2002-424161).

With respect to claim 1, Kim discloses, in Figure 1, a data output circuit comprising a) a first inversion unit [100] for receiving a first data signal [Din] of an operating voltage level and inverting the received first data signal to obtain a first inverted data signal [input of MP23]; b) a first voltage compensation unit [104] for compensating for the voltage level of the first inverted data signal to obtain a first driving signal, when a first power supply voltage of an output voltage level is different from a second power supply voltage of the operating voltage level by at least a predetermined voltage level; c) a second inversion unit [102] for receiving a second data signal with the operating voltage level and inverting the received second data signal to obtain a second

inverted data signal; d) a second voltage compensation unit [106] for compensating for the voltage level of the second inverted data signal to obtain a second driving signal, when the levels of the first and second power supply voltages are different by at least a predetermined voltage level; e) a driver unit [108] for receiving the first and second driving signal and outputting an output data signal of a logic level that is opposite the logic levels of the first and second driving signals.

With respect to claim 2, Kim discloses, in Figure 1, that the first inversion unit forms an inverter comprising a first PMOS transistor [MP20] and a first NMOS transistor [MN20] serially connected between the first power supply voltage and a first ground voltage of the output voltage level, and wherein the first data signal is applied to a gate of the first PMOS transistor and a gate of the first NMOS transistor.

With respect to claim 3, Kim discloses, in Figure 1, that the second inversion unit [102] forms an inverter comprising a second PMOS transistor [MP21] and a second NMOS transistor [MN21] serially connected between the first power supply voltage and a first ground voltage of The output voltage level, and wherein the second data signal is applied to a gate of the second PMOS transistor and a gate of the second NMOS transistor.

With respect to claim 8, Kim discloses, in Figure 1, that the first and second data signals have the same level.

With respect to claim 13, Kim discloses, in Figure 1, a data output circuit comprising a) a first inversion unit [100] for receiving a first data signal [Din] of an operating voltage level and inverting the received first data signal to obtain a first inverted data signal, when an output voltage level of a first power supply voltage is equal to an operating voltage level of a second

power supply voltage; b) a first voltage compensation unit [104] for compensating for the voltage level of the first inverted data signal to obtain a first driving signal, when the levels of the first and second power supply voltages are different by at least a predetermined voltage level; c) a second inversion unit [102] for receiving a second data signal of the operating voltage level and inverting the received second data signal to obtain a second inverted data signal, when the levels of the first and second power supply voltages are the same; d) a second voltage compensation unit [106] for compensating for the voltage level of the second inverted data signal to obtain a second driving signal, when the levels of the first and second power supply voltages are different by at least a predetermined voltage level; and e) a driver unit [108] for receiving the first and second driving signals and outputting an output data signal of a logic level that is opposite the logic levels of the first and second driving signals.

With respect to claim 22, Kim discloses, in Figure 1, that the first and second data signals have the same level.

Allowable Subject Matter

7. Claims 23-30 would be allowed if corrected to overcome the objection set forth in this office action.

8. Claims 4-7, 9-12, and 14-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

• The first voltage compensation unit comprises a) a first compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage, and b) a second compensation PMOS transistor, a source of which is connected to the drain of the first compensation PMOS transistor, a gate of which is subjected to the first data signal, ant a drain of which is connected to a connection node between the first PMOS transistor and the first NMOS transistor, as called for in claims 4 and 16;

• The second voltage compensation unit comprises a) a third compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage, and b) a fourth compensation PMOS transistor, a source of which is connected to the drain of the third compensation PMOS transistor, a gate of which is subjected to the second data signal, and a drain of which is connected to a connection node between the second PMOS transistor and the second NMOS transistor, as called for in claims 6 and 20;

• The first voltage compensation unit comprises a) a first compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to a first drop voltage; b) a second compensation PMOS transistor, a source of which is connected to the drain of the first compensation PMOS transistor, a gate of which is subjected to the firs data signal, and a drain of which is connected to a connection node between the first PMOS transistor and the first NMOS transistor; c) first through N-th load PMOS transistors serially connected to the first power supply voltage; and d) a first load NMOS transistor connected between the N-th load PMOS transistor and a second ground voltage, a drain of which

generates the first drop voltage and a gate and a source of which are connected to each other, as called for in claim 9;

- The second voltage compensation unit comprises a) a third compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to a second drop voltage, and b) a fourth compensation PMOS transistor, a source of which is connected to the drain of the third compensation PMOS transistor, a gate of which is subjected to the second data signal, and a drain of which is connected to a connection node between the second PMOS transistor and the second NMOS transistor, as called for in claim 11;

- The first inversion unit comprises a first control voltage generation unit for generating the first control voltage to have a first logic level, when the levels of the first and second power supply voltages are the same, and generating the first control voltage to have a second logic level, when the level of the first power supply voltage is less than that of the second power supply voltage by a predetermined voltage level, as called for in claim 14;

- The second inversion unit comprises a second control voltage generation unit generating the second control voltage to have a first logic level, when the levels of the first and second power supply voltages are the same, and generating the second control voltage to have a second logic level, when the level of the first power supply voltage is less than that of the second power supply voltage by a predetermined voltage level, as called for in claim 18; and

- A second control unit generating a third control signal for controlling the operation of the second voltage compensation unit if the levels of the first and second power supply voltages are the same and generating a fourth control signal for controlling the operation of the second inversion unit if the levels of the first and second power supply

voltages are different by at least a predetermined voltage level, in combination with the remaining claimed limitations, as called for in claim 23.

Citation of Relevant Prior Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Tomita (U.S. Patent No. 6,559,676) discloses an output buffer circuit including first and second MOS transistors connected in series between a power supply and ground.

Prior art Bryan et al. (U.S. Patent No. 6,169,421) discloses a complementary metal-oxide semiconductor buffer.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Examiner
Art Unit 2816

LMN